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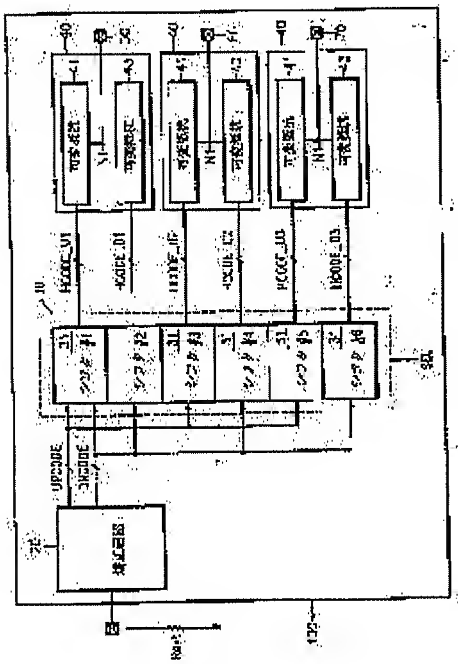
(54) **ACTIVE TERMINAL RESISTANCE VALUE CALIBRATING CIRCUIT, MEMORY CHIP AND ACTIVE TERMINAL RESISTANCE CALIBRATING METHOD**



(57)Abstract:

PROBLEM TO BE SOLVED: To provide a calibrating method that can calibrate a terminal resistance value insensibly to a process, voltage or temperature change.

SOLUTION: The calibrating method has a step (a) of calibrating the resistance value of a first variable resistance to the resistance value of an external resistance and calibrating the resistance value of a second variable resistance to the resistance value of the first variable resistance, and a step (b) of calibrating the resistance value of an active terminal resistance to the resistance value of the external resistance. The step (a) has a step of calibrating the resistance value of the first variable resistance to the resistance value of the external resistance in response to a first control code and calibrating the resistance value of the second variable resistance to the resistance value of the first variable resistance in response to a second control code. The first control code is generated according to the compared result of the resistance values of the first variable resistance and external resistance, and the second control code is generated according to the compared result of the resistance values

of the first variable resistance and second variable resistance. The step (a) has a step wherein the resistance value of the first variable resistance and the resistance value of the second variable resistance increase/decrease at the same time.

CLAIMS

[Claim(s)]

[Claim 1] The resistance calibration approach of the active terminator characterized by having the phase which proofreads the resistance of the 2nd variable resistance to the resistance of said 1st variable resistance, and the phase which proofreads the resistance of the (b) aforementioned active terminator to the resistance of said external resistance in the approach of proofreading the resistance of an active terminator while proofreading the resistance of the (a) 1st variable resistance to the resistance of external resistance.

[Claim 2] The aforementioned (a) phase is the resistance calibration approach of the active terminator according to claim 1 characterized by including the phase which answers the 2nd control code and proofreads the resistance of said 2nd variable resistance to the resistance of said 1st variable resistance while answering the 1st control code and proofreading the resistance of said 1st variable resistance to the resistance of said external resistance.

[Claim 3] The resistance calibration approach of the active terminator according to claim 2 characterized by having the phase of generating said 1st control code according to the comparison result of the resistance of said 1st variable resistance, and the resistance of said external resistance, and generating said 2nd control code according to

the comparison result of the resistance of said 1st variable resistance, and the resistance of said 2nd variable resistance.

[Claim 4] The aforementioned (a) phase is the resistance calibration approach of the active terminator according to claim 1 characterized by including the phase which the resistance of said 1st variable resistance and the resistance of said 2nd resistance fluctuate simultaneously.

[Claim 5] The phase which compares the electrical potential difference and reference voltage of the pad to which external resistance is connected in the approach of proofreading the resistance of an active terminator, and outputs the 1st comparison signal corresponding to the comparison result, The phase which proofreads the resistance of the 1st variable resistance to the resistance of said external resistance until it answers said 1st comparison signal and the electrical potential difference of said pad becomes the same as that of said reference voltage, The phase which compares the electrical potential difference of said pad with the electrical potential difference of the 2nd variable resistance, and outputs the 2nd comparison signal corresponding to the comparison result, The resistance calibration approach of the active terminator characterized by having the phase which answers said 2nd comparison signal and proofreads the resistance of the 2nd variable resistance to the resistance of said external resistance, and the phase which proofreads the resistance of said active terminator to said 1st variable-resistance value and/or the resistance of said 2nd variable resistance.

[Claim 6] The electrical potential difference of said pad is the resistance calibration approach of the active terminator according to claim 5 characterized by being generated according to the current which passes said 1st variable resistance.

[Claim 7] The electrical potential difference of the 2nd variable

resistance is the resistance calibration approach of the active terminator according to claim 5 characterized by being generated according to the current which flows to the same dummy variable resistance as said 1st variable resistance.

[Claim 8] The resistance calibration approach of the active terminator according to claim 5 characterized by the resistance of said 1st variable resistance and the resistance of said 2nd resistance fluctuating simultaneously.

[Claim 9] In the calibration circuit which proofreads the resistance of an active terminator to the resistance of external resistance The 1st control circuit which outputs the 1st control code which controls the resistance of the 1st variable resistance which compares the electrical potential difference and reference voltage of the 1st node to which external resistance is connected, and supplies a current to said 1st node, The electrical potential difference of the 2nd node to which the 2nd variable resistance is connected is compared with the electrical potential difference of said 1st node. It has the 2nd control circuit which outputs the 2nd control code which controls the resistance of the same dummy variable resistance as said 1st variable resistance which supplies a current to said 2nd node. While the resistance of said 1st variable resistance and the resistance of said dummy variable resistance answer said 1st control code and are proofread by the resistance of said external resistance The resistance of said 2nd variable resistance answers said 2nd control code, and is proofread by the resistance of said external resistance. The resistance of said active terminator is the resistance calibration circuit of the active terminator characterized by answering said 1st control code and/or said 2nd control code, and being proofread by the resistance of said external resistance.

[Claim 10] The resistance of said 1st variable resistance and the

resistance of said 2nd variable resistance are the resistance calibration circuit of the active terminator according to claim 9 characterized by fluctuating simultaneously.

[Claim 11] It is the resistance calibration circuit of the active terminator according to claim 9 characterized by producing the electrical potential difference of said 1st node according to the current which flows to said 1st variable resistance, and producing the electrical potential difference of said 2nd node according to the current which flows to said dummy variable resistance.

[Claim 12] In the calibration circuit which proofreads the resistance of an active terminator to the resistance of external resistance The 1st control-code generating circuit which compares with the electrical potential difference and reference voltage of said 1st node the 1st node to which said external resistance and 1st variable resistance are connected, and outputs the 1st control code corresponding to the comparison result, The 2nd node to which the dummy variable resistance and the 2nd variable resistance which have the same resistance as the resistance of said 1st variable resistance are connected, It has the 2nd control-code generating circuit which compares the electrical potential difference of said 1st node with the electrical potential difference of said 2nd node, and outputs the 2nd control code corresponding to the comparison result. While the resistance of said 1st variable resistance and the resistance of said dummy variable resistance answer said 1st control code and are proofread by the resistance of said external resistance The resistance of said 2nd variable resistance answers said 2nd control code, and is proofread by the resistance of said external resistance. The resistance of said active terminator is the resistance calibration circuit of the active terminator characterized by answering said 1st control code and/or said

2nd control code, and being proofread by the resistance of said external resistance.

[Claim 13] The resistance of said 1st variable resistance and the resistance of said 2nd variable resistance are the resistance calibration circuit of the active terminator according to claim 12 characterized by fluctuating simultaneously.

[Claim 14] It is the resistance calibration circuit of the active terminator according to claim 12 characterized by producing the electrical potential difference of said 1st node according to the current which flows to said 1st variable resistance, and producing the electrical potential difference of said 2nd node according to the current which flows to said dummy variable resistance.

[Claim 15] The calibration circuit which outputs the 1st control code and the 2nd control code in a memory apparatus, The shift block which outputs the control code for answering a selection signal, said 1st control code and said 2nd control code, and controlling the resistance of an active terminator, Said control code is answered and it has the variable-resistance section which proofreads the resistance of said active terminator in agreement with the resistance of the external resistance connected to said calibration circuit. Said calibration circuit The 1st node to which said external resistance and 1st variable resistance are connected, and the 1st control-code generating circuit which compares the electrical potential difference and reference voltage of said 1st node, and outputs said 1st control code corresponding to the comparison result, The 2nd node to which the dummy variable resistance and the 2nd variable resistance which have the same resistance as the resistance of said 1st variable resistance are connected, It has the 2nd control-code generating circuit which compares the electrical potential difference of said 1st node, and the

electrical potential difference of said 2nd node, and outputs said 2nd control code corresponding to the comparison result. It is the memory apparatus characterized by for the resistance of said 2nd variable resistance answering said 2nd control code while the resistance of said 1st variable resistance and the resistance of said dummy variable resistance answer said 1st control code and being proofread by the resistance of said external resistance, and being proofread by the resistance of said external resistance.

[Claim 16] The resistance of said 1st variable resistance and the resistance of said 2nd variable resistance are a memory apparatus according to claim 15 characterized by fluctuating simultaneously.

[Claim 17] It is the memory apparatus according to claim 15 characterized by producing the electrical potential difference of said 1st node according to the current which flows to said 1st variable resistance, and producing the electrical potential difference of said 2nd node according to the current which flows to said dummy variable resistance.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the termination of a bus and relates to the memory apparatus which equips a detail with the calibration circuit which can proofread the resistance of active termination regardless of change of a process, an electrical potential difference, or temperature, its approach, and said calibration circuit more.

[0002]

[Description of the Prior Art] Generally, SSTL (stub busTerminated logic)

and active termination (active termination) are used by the memory system for the termination of a bus. Active termination is also called termination (on-chip termination) on chip, and performs termination of a bus using the active terminator inside a chip (the following, "terminator"). Active termination has good signal transfer characteristics, and its data rate is higher than SSTL.

[0003] It is the key point of active termination how the resistance (the following, "terminator value") of a terminator can be proofread to the resistance of the request to accuracy. Although the analog-control electrical potential difference was used as a control signal for conventionally proofreading a terminator value, since an analog-control electrical potential difference is sensitive to a noise, it has the trouble which cannot proofread a terminator value to accuracy. Moreover, since control voltage was sensitive to the noise, there was a trouble that the signal transfer characteristics of a bus fell.

[0004] When sharing two chips and carrying out active termination (the following, "x2"), or to share four chips and carry out active termination (the following, "x4"), other calibration circuits for proofreading a terminator value compared with the case (the following, "x1") where active termination is carried out, with one chip are required for an addition target. Therefore, the overhead of the increase of the power consumption for active termination and layout area is quite large conventionally.

[0005]

[Problem(s) to be Solved by the Invention] Therefore, the technical technical problem which this invention tends to solve is offering the memory apparatus which equips change of a process, an electrical potential difference, or temperature with the calibration circuit which can proofread a terminator value insensibly, its approach, and said

calibration circuit.

[0006] Moreover, other technical technical problems which this invention tends to solve are offering the memory apparatus for embodying an approach being able to carry out overhead reduction of power consumption and the layout area, and this.

[0007]

[Means for Solving the Problem] The approach of proofreading the resistance of the active terminator for attaining said technical technical problem is characterized by having the phase which proofreads the resistance of the 2nd variable resistance to the resistance of said 1st variable resistance while proofreading the resistance of the (a) 1st variable resistance to the resistance of external resistance, and the phase which proofreads the resistance of the (b) aforementioned active terminator to the resistance of said external resistance.

[0008] For example,. the aforementioned (a) phase includes the phase which answers the 2nd control code and proofreads the resistance of said 2nd variable resistance to the resistance of said 1st variable resistance while it answers the 1st control code and proofreads the resistance of said 1st variable resistance to the resistance of said external resistance.

[0009] For example, it is ** which produces said 1st control code according to the comparison result of the resistance of said 1st variable resistance, and the resistance of said external resistance, and produces said 2nd control code according to the comparison result of the resistance of said 1st variable resistance, and the resistance of said 2nd variable resistance.

[0010] For example, the aforementioned (a) phase includes the phase which the resistance of said 1st variable resistance and the resistance of said 2nd resistance fluctuate simultaneously.

[0011] The approach of proofreading the resistance of other active terminators for attaining said technical technical problem The phase which compares the electrical potential difference and reference voltage of the pad to which external resistance is connected, and outputs the 1st comparison signal corresponding to the comparison result, The phase which proofreads the resistance of the 1st variable resistance to the resistance of said external resistance until it answers said 1st comparison signal and the electrical potential difference of said pad becomes the same as that of said reference voltage, The phase which compares the electrical potential difference of said pad with the electrical potential difference of the 2nd variable resistance, and outputs the 2nd comparison signal corresponding to the comparison result, It is characterized by having the phase which answers said 2nd comparison signal and proofreads the resistance of the 2nd variable resistance to the resistance of said external resistance, and the phase which proofreads the resistance of said active terminator to said 1st variable-resistance value and/or the resistance of said 2nd variable resistance.

[0012] For example, the electrical potential difference of said pad is produced according to the current which passes said 1st variable resistance.

[0013] For example, the electrical potential difference of said 2nd variable resistance is produced according to the current which flows to the same dummy variable resistance as said 1st variable resistance.

[0014] For example, the resistance of said 1st variable resistance and the resistance of said 2nd resistance are fluctuated simultaneously.

[0015] For example, the calibration circuit which proofreads the resistance of the active terminator for attaining said technical technical problem to the resistance of external resistance The 1st control circuit

which outputs the 1st control code which controls the resistance of the 1st variable resistance which compares the electrical potential difference and reference voltage of the 1st node to which external resistance is connected, and supplies a current to said 1st node, It has the 2nd control circuit which outputs the 2nd control code which controls the resistance of the same dummy variable resistance as said 1st variable resistance which compares with the electrical potential difference of said 1st node the electrical potential difference of the 2nd node to which the 2nd variable resistance is connected, and supplies a current to said 2nd node. While the resistance of said 1st variable resistance and the resistance of said dummy variable resistance answer said 1st control code and are proofread by the resistance of said external resistance It is characterized by the resistance of said 2nd variable resistance answering said 2nd control code, and being proofread by the resistance of said external resistance, and for the resistance of said active terminator answering said 1st control code and/or said 2nd control code, and being proofread by the resistance of said external resistance.

[0016] For example, the resistance of said 1st variable resistance and the resistance of said 2nd variable resistance are fluctuated simultaneously.

[0017] For example, it is characterized by producing the electrical potential difference of said 1st node according to the current which flows to said 1st variable resistance, and producing the electrical potential difference of said 2nd node according to the current which flows to said dummy variable resistance.

[0018] The calibration circuit which proofreads the resistance of other active terminators for attaining said technical technical problem to the resistance of external resistance The 1st control-code generating circuit

which compares with the electrical potential difference and reference voltage of said 1st node the 1st node to which said external resistance and 1st variable resistance are connected, and outputs the 1st control code corresponding to the comparison result, The 2nd node to which the dummy variable resistance and the 2nd variable resistance which have the same resistance as the resistance of said 1st variable resistance are connected, It has the 2nd control-code generating circuit which compares the electrical potential difference of said 1st node with the electrical potential difference of said 2nd node, and outputs the 2nd control code corresponding to the comparison result. While the resistance of said 1st variable resistance and the resistance of said dummy variable resistance answer said 1st control code and are proofread by the resistance of said external resistance It is characterized by the resistance of said 2nd variable resistance answering said 2nd control code, and being proofread by the resistance of said external resistance, and for the resistance of said active terminator answering said 1st control code and/or said 2nd control code, and being proofread by the resistance of said external resistance.

[0019] For example, the resistance of said 1st variable resistance and the resistance of said 2nd variable resistance are fluctuated simultaneously.

[0020] For example, the electrical potential difference of said 1st node is produced according to the current which flows to said 1st variable resistance, and the electrical potential difference of said 2nd node is produced according to the current which flows to said dummy variable resistance.

[0021] The memory apparatus for attaining said technical technical problem MARUCHIPUREKKUSHINGU [answer the calibration circuit which outputs the 1st control code and the 2nd control code, and a

selection signal, and / said 1st control code and said 2nd control code] The shift block which outputs the control code for controlling the resistance of an active terminator, Said control code is answered and it has the variable-resistance section which proofreads the resistance of said active terminator in agreement with the resistance of the external resistance connected to said calibration circuit. Said calibration circuit The 1st node to which said external resistance and 1st variable resistance are connected, and the 1st control-code generating circuit which compares the electrical potential difference and reference voltage of said 1st node, and outputs said 1st control code corresponding to the comparison result, The 2nd node to which the dummy variable resistance and the 2nd variable resistance which have the same resistance as the resistance of said 1st variable resistance are connected, It has the 2nd control-code generating circuit which outputs said 2nd control code which compares the electrical potential difference of said 1st node, and the electrical potential difference of said 2nd node, and ****s in the comparison result. While the resistance of said 1st variable resistance and the resistance of said dummy variable resistance answer said 1st control code and being proofread by the resistance of said external resistance, it is characterized by for the resistance of said 2nd variable resistance answering said 2nd control code, and being proofread by the resistance of said external resistance.

[0022] For example, the resistance of said 1st variable resistance and the resistance of said 2nd variable resistance are fluctuated simultaneously.

[0023] For example, the electrical potential difference of said 1st node is produced according to the current which flows to said 1st variable resistance, and the electrical potential difference of said 2nd node is produced according to the current which flows to said dummy variable

resistance.

[0024]

[Embodiment of the Invention] By explaining the desirable operation gestalt of this invention with reference to the attached drawing hereafter explains this invention to a detail. The same reference mark which each drawing was shown shows the same component.

[0025] Drawing 1 shows roughly the block diagram of a memory apparatus equipped with the active terminator calibration circuit of the desirable operation gestalt of this invention. A chip 100 will be equipped with the active resistance calibration circuit (the following, "calibration circuit") 20, the shift block 30, much variable-resistance sections 40, and many pads 50, 60, and 70 if drawing 1 is referred to. The calibration circuit 20 is connected with external resistance Rext through a pad 10.

[0026] The calibration circuit 20 outputs the 1st control-code UPCODE and the 2nd control-code DNCODE to the shift block 30. The 1st control-code UPCODE and the 2nd control-code DNCODE consist of for example, N bits.

[0027] The shift block 30 is equipped with two or more shifters 31, answers a selection signal SEL, and outputs control-code HCODE_Ui and HCODE_Di (i is 1 thru/or 3 here) which control the terminator value for x1, x2, or x4 to two or more variable-resistance sections 40. Control-code HCODE_Ui and HCODE_Di consist of for example, N bits.

[0028] Therefore, a shifter 31 shifts 1st/2nd control-code UPCODE/DNCODE 1 time or more than it, and has the advantage in which the terminator value for x2 or x4 can be generated.

[0029] Each of two or more variable-resistance sections 40 is equipped with the 1st variable resistance 41 and the 2nd variable resistance 43, it answers control-code HCODE_Ui and HCODE_Di, and it proofreads a terminator value so that it may be made in agreement with the resistance

of external resistance Rext. A pad 50 is a pad for data output, a pad 60 is a pad for a clock signal, and a pad 70 is a pad for for example, the address / instruction signal. each of two or more pads 50, 60, and 70 -- two or more variable-resistance sections 40 -- it connects with each node N1.

[0030] Drawing 2 shows the circuit diagram of the calibration circuit of the desirable operation gestalt of this invention. If drawing 2 is referred to, the calibration circuit 20 will be equipped with the comparison circuits 21 and 23 of the 1st variable resistance 41, the dummy variable resistance 42, and the 2nd 43 or 2 variable resistance, the 1st control-code generating circuit 25, and the 2nd control-code generating circuit 27.

[0031] The 1st variable resistance 41 is connected between the 1st power source VDDQ and a pad 10, the dummy variable resistance 42 is connected between the 1st power source VDDQ and a node N3, and the 2nd variable resistance 43 is connected between a node N3 and the 2nd power source VSSQ. The structure of the dummy variable resistance 42 and actuation are the same as the structure of the 1st variable resistance 41, and actuation, and the actuation is the same, although it has symmetrical structure mutually as indicated in drawing 5 as the dummy variable resistance 42 and the 2nd variable resistance 43.

[0032] A comparison circuit 21 compares reference voltage VREF with the electrical potential difference of a pad 10, and outputs 1st comparison signal UP_COMP corresponding to the comparison result to the 1st control-code generating circuit 25. The electrical potential difference of a pad 10 changes with the currents which flow to the 1st variable resistance 41.

[0033] A comparison circuit 23 compares the electrical potential difference of a node N3 with the electrical potential difference of a pad

10, and outputs 2nd comparison signal DN_COMP corresponding to the comparison result to the 2nd control-code generating circuit 27. The electrical potential difference of a node N3 changes with the currents which flow through the dummy variable resistance 42. As for reference voltage VREF and the electrical potential difference of a node N3, it is desirable that it is 0.5VDDQ.

[0034] The 1st control-code generating circuit 25 answers 1st comparison signal UP_COMP, and outputs the 1st control-code UPCODE to the 1st variable resistance 41, the dummy variable resistance 42, and the shift block 30. When the resistance of the 1st variable resistance 41 and the resistance of the dummy variable resistance 42 answer the 1st control-code UPCODE and are proofread identically to the resistance of external resistance Rext, reference voltage VREF and the electrical potential difference of a pad 10 become the same. Since it consists of general up/down counters, the 1st control-code generating circuit 25 omits detailed explanation.

[0035] The 2nd control-code generating circuit 27 answers 1st comparison signal UP_COMP and 2nd comparison signal DN_COMP, and outputs the 2nd control-code DNCODE to the 2nd variable resistance 43 and the shift block 30. When the resistance of the 2nd variable resistance 43 answers the 2nd control-code DNCODE and is proofread identically to the resistance of the dummy variable resistance 42, the electrical potential difference of a node N3 and the electrical potential difference of a pad 10 become the same.

[0036] Drawing 3 shows the block diagram of the 2nd control-code generating circuit of drawing 2 . If drawing 3 is referred to, the 2nd control-code generating circuit 27 will be equipped with a logic gate 28 and an up/down counter 29. A logic gate 28 is an exclusive-NOR operation (Exclusive-NOR) circuit, an up/down counter 29 answers the

output signal of a logic gate 27, and it enables it. That is, since an up/down counter 29 answers 1st comparison signal UP_COMP and 2nd comparison signal DN_COMP which have the 1st condition (or the 2nd condition) and they enable it, the quantization error produced by digital calibration decreases.

[0037] The case where it is proofread so that the resistance of the 1st variable resistance 41 and the resistance of the 2nd variable resistance 43 may be in agreement with the resistance of external resistance Rext with reference to drawing 1 thru/or drawing 3 is explained.

[0038] First, the electrical potential difference of a pad 10 is determined by the current which flows to the 1st variable resistance 41. When the electrical potential difference of a pad 10 is larger than reference voltage VREF (namely, when the resistance of the 1st variable resistance 41 is smaller than the resistance of external resistance Rext), A comparison circuit 21 outputs 1st comparison signal UP_COMP of the 1st condition, and since down counting of the 1st control-code generating circuit 25 which consists of up/down counters is answered and carried out to 1st comparison signal UP_COMP of the 1st condition, the 1st control-code UPCODE decreases.

[0039] Therefore, the resistance of the 1st variable resistance 41 and the resistance of the dummy variable resistance 42 answer and increase to the 1st control-code UPCODE. Since it is repetitively carried out until the electrical potential difference and reference voltage VREF of a pad 10 become the same, such actuation is proofread after all so that the resistance of the 1st variable resistance 41 and the resistance of the dummy variable resistance 42 may do to the resistance of external resistance Rext one.

[0040] Since a comparison circuit 21 outputs 1st comparison signal UP_COMP of the 2nd condition and rise counting of the 1st control-code

generating circuit 25 is answered and carried out to 1st comparison signal UP_COMP of the 2nd condition when the electrical potential difference of a pad 10 is smaller than reference voltage VREF (namely, when the resistance of the 1st variable resistance 41 is larger than the resistance of external resistance Rext), the 1st control-code UPCODE increases.

[0041] Therefore, the resistance of the 1st variable resistance 41 and the resistance of the dummy variable resistance 42 answer the 1st control-code UPCODE, and decrease. Since it is repetitively carried out until the electrical potential difference and reference voltage VREF of a pad 10 become the same, such actuation is proofread after all so that the resistance of the 1st variable resistance 41 and the resistance of the dummy variable resistance 42 may be in agreement with the resistance of external resistance Rext.

[0042] Next, the electrical potential difference of a node N3 is determined by the current which flows to the dummy variable resistance 42, and when the electrical potential difference of a pad 10 is larger than the electrical potential difference of a node N3, a comparison circuit 23 outputs 2nd comparison signal DN_COMP of the 1st condition (namely, when the resistance of the 2nd variable resistance 43 is smaller than the resistance of the 1st variable resistance 41 or the dummy variable resistance 42).

[0043] Since the 2nd control-code DNCODE by which down counting was answered and carried out to 1st comparison signal UP_COMP of the 1st condition and 2nd comparison signal DN_COMP of the 1st condition is outputted to the 2nd variable resistance 43, the 2nd control-code generating circuit 27 increases the resistance of the 2nd variable resistance 43 until it answers the 2nd control-code DNCODE and becomes the same as that of the resistance of the dummy variable

resistance 42.

[0044] When the electrical potential difference of a pad 10 is smaller than the electrical potential difference of a node N3, a comparison circuit 23 outputs 2nd comparison signal DN_COMP of the 2nd condition (namely, when the resistance of the 2nd variable resistance 43 is larger than the resistance of the dummy variable resistance 42). Since the 2nd control-code generating circuit 27 outputs the 2nd control-code DNCODE by which rise counting was answered and carried out to 1st comparison signal UP_COMP of the 2nd condition, and 2nd comparison signal DN_COMP of the 2nd condition to the 2nd variable resistance 43, they decrease in number until the resistance of the 2nd variable resistance 43 answers the 2nd control-code DNCODE and becomes the same as that of the resistance of the dummy variable resistance 42.

[0045] That is, since the calibration circuit 20 makes the resistance of variable resistance 41, 42, and 43 fluctuate simultaneously regardless of a process, an electrical potential difference, or temperature through the above-mentioned process, the resistance of variable resistance 41, 42, and 43 is proofread by the resistance of external resistance Rext. Moreover, also when comparison circuits 21 and 23 have offset, the electrical potential difference of a pad 10, the electrical potential difference of a node N3, and reference voltage VREF become the same according to the above-mentioned process.

[0046] That is, since the calibration circuit 20 of the desirable operation gestalt of this invention can compensate change of the termination voltage by offset of comparators 21 and 23, it can make the timing margin at the time of high-speed operation increase.

[0047] Drawing 4 shows the circuit diagram of the shifter of drawing 1 . A shifter 31 will be equipped with two or more multi-PUREKKUSA 33 if drawing 4 is referred to. Multi-PUREKKUSA 33 answers the selection

signal SEL of N bit, 1st/2nd control-code UPCODE/DNCODE, and outputs control-code HCODE_Ui and HCODE_Di (i is 1 thru/or 3 here) which control the terminator value for x1, x2, or x4.

[0048] While in the case of xtwo shifter #3 and #4 answer a selection signal SEL and same control-code HCODE_U2/HCODE_D2 as 1st/2nd control-code UPCODE/DNCODE is outputted, shifter #5 and #6 output control-code HCODE_U3/HCODE_D3 which answered the selection signal SEL and shifted 1st/2nd control-code UPCODE/DNCODE once.

[0049] Drawing 5 shows the circuit diagram of the variable-resistance section of drawing 1 . The 1st variable resistance 41 and the dummy variable resistance 42 are equipped with two or more PMOS transistors, two or more resistance R, 21R and 22R, ..., 2NR, and each transistor is connected to each resistance and serial. Control-code HCODE_Ui and HCODE_Di (here, i is 1 thru/or 3) are the codes by which weighting was carried out with binary, and are inputted into the gate of a corresponding transistor. Each resistance has the resistance by which weighting was carried out as shown in drawing 5 .

[0050] The 1st variable resistance 41 and the dummy variable resistance 42 function as resistance which has the resistance corresponding to control-code HCODE_Ui and HCODE_Di (it is here and i is 1 thru/or 3). That is, the resistance of xone and the resistance of xtwo differ from the resistance of xfour mutually.

[0051] The 2nd variable resistance 43 is equipped with two or more NMOS transistors, two or more resistance R, 21R and 22R, ..., 2NR, and each transistor is connected to each resistance and serial. Control-code HCODE_Di and HCODE_Di (here, i is 1 thru/or 3) are the codes by which weighting was carried out with binary, and are inputted into the gate of a corresponding transistor. Each resistance has the resistance by which weighting was carried out as shown in drawing 5 .

[0052] The chip 100 of the desirable operation gestalt of this invention can shift 1st/2nd control-code UPCODE/DNCODE using one calibration circuit 20 and shifter 31, and can generate simultaneously the terminator value for x2 or x4. Therefore, the chip 100 of the desirable operation gestalt of this invention has the advantage in which power consumption can be decreased, and is effective in the ability to decrease the overhead of layout area.

[0053] Although the desirable operation gestalt shown in the drawing was explained by reference, this invention does not pass over this to an instantiation-thing, but if it is this contractor of this technical field, it will be able to understand the point that deformation various from now on and other equal operation gestalten are possible. Therefore, the true technical protection range of this invention should be decided by technical thought of a claim.

[0054]

[Effect of the Invention] The calibration circuit and the proofreading method by this invention have the advantage in which the resistance of a terminator can be proofread regardless of a process, an electrical potential difference, or temperature.

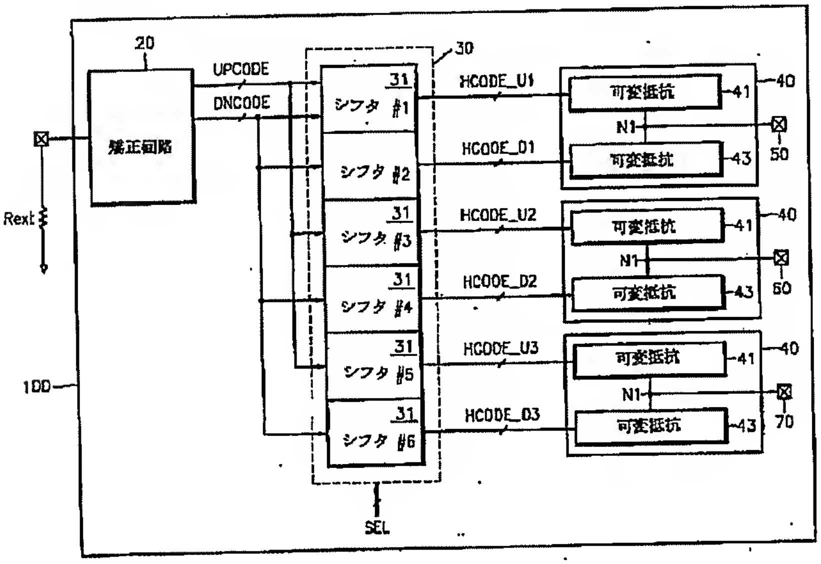
[0055] And the calibration circuit and the calibration approach by this invention have the advantage in which the resistance over a noise can be strengthened. And the calibration circuit and the calibration approach by this invention have the advantage in which the termination of a bus is easily controllable.

[0056] Moreover, the calibration circuit and the calibration approach by this invention can decrease the quantization error by digital control. Furthermore, the memory apparatus by this invention decreases power consumption, can enlarge the timing margin at the time of high-speed operation, and has the advantage in which the overhead of layout area

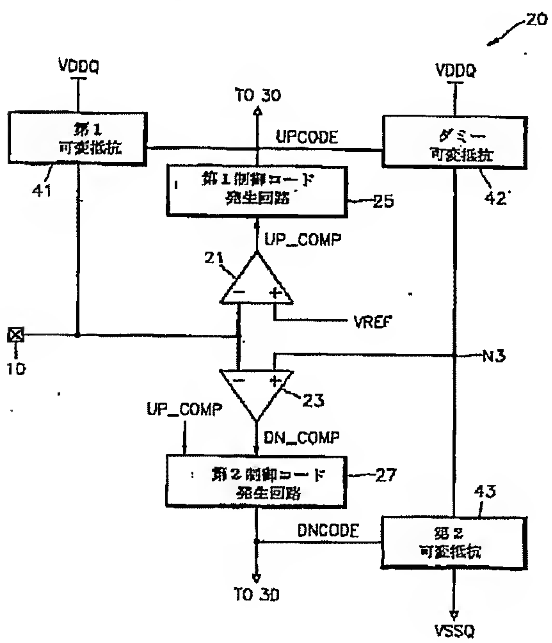
can be decreased.

DRAWINGS

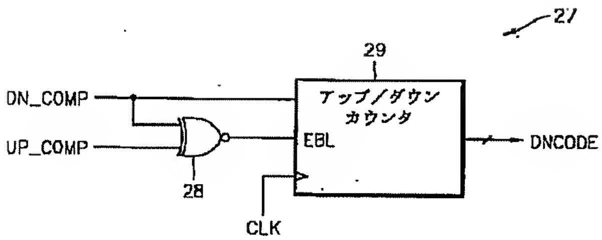
[Drawing 1]



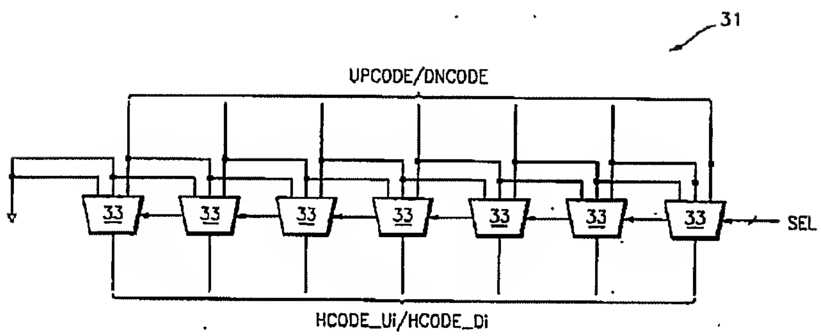
[Drawing 2]



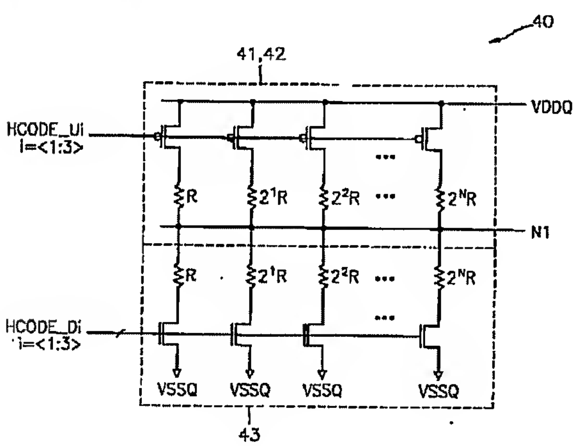
[Drawing 3]



[Drawing 4]



[Drawing 5]



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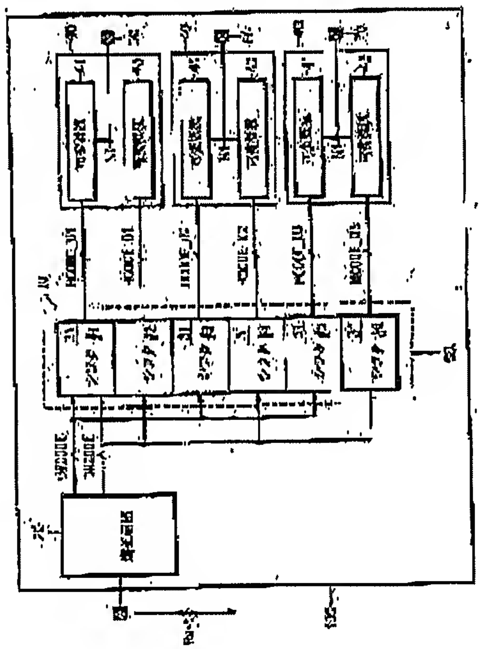
(54) ACTIVE TERMINAL RESISTANCE VALUE CALIBRATING CIRCUIT, MEMORY CHIP AND ACTIVE TERMINAL RESISTANCE CALIBRATING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a calibrating method that can calibrate a terminal resistance value insensibly to a process, voltage or temperature change.
SOLUTION: The calibrating method has a step (a) of calibrating the resistance value of a first variable resistance to the resistance value of an external resistance and calibrating the resistance value of a second variable resistance to the resistance value of the first variable resistance, and a step (b) of calibrating the resistance value of an active terminal resistance to the resistance value of the external resistance. The step (a) has a step of calibrating the resistance value of the first variable resistance to the resistance value of the external resistance in response to a first control code and calibrating the resistance value of the second variable resistance to the resistance value of the first variable resistance in response to a second control code. The first control code is generated according to the compared result of the resistance values of the first variable resistance and external resistance, and the second control code is generated according to the compared result of the resistance values of the first variable resistance and second variable resistance. The step (a) has a step wherein the resistance value of the first variable resistance and the resistance value of the second variable resistance increase/decrease at the same time.



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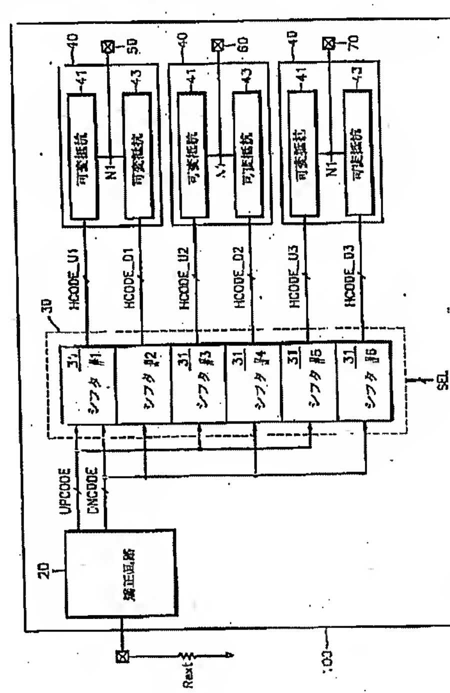
最終頁に続く

(54)【発明の名称】　能動終端抵抗値較正回路、メモリチップ及び能動終端抵抗較正方法

(57)【要約】
【課題】工程、電圧、または温度の変化に鈍感に終端抵抗値を較正できる較正方法を提供する。
【解決手段】（ａ）第１可変抵抗の抵抗値を外部抵抗の抵抗値に較正すると共に、第２可変抵抗の抵抗値を前記第１可変抵抗の抵抗値に較正する段階と、（ｂ）前記能動終端抵抗の抵抗値を前記外部抵抗の抵抗値に較正する段階とを備える。前記（ａ）段階は第１制御コードに応答して前記第１可変抵抗の抵抗値を前記外部抵抗の抵抗値に較正すると共に、第２制御コードに応答して前記第２可変抵抗の抵抗値を前記第１可変抵抗の抵抗値に較正する段階を備える。前記第１制御コードは前記第１可変抵抗の抵抗値と前記外部抵抗の抵抗値との比較結果に応じて生じ、前記第２制御コードは前記第１可変抵抗の抵抗値と前記第２可変抵抗の抵抗値との比較結果に応じて生じる。前記（ａ）段階は前記第１可変抵抗の抵抗値と前記第２抵抗の抵抗値とが同時に増減する段階を備える。



【特許請求の範囲】

【請求項１】 能動終端抵抗の抵抗値を較正する方法において、

（ａ）第１可変抵抗の抵抗値を外部抵抗の抵抗値に較正すると共に、第２可変抵抗の抵抗値を前記第１可変抵抗の抵抗値に較正する段階と、

（ｂ）前記能動終端抵抗の抵抗値を前記外部抵抗の抵抗値に較正する段階とを備えることを特徴とする能動終端抵抗の抵抗値較正方法。

【請求項２】 前記（ａ）段階は、第１制御コードに応答して前記第１可変抵抗の抵抗値を前記外部抵抗の抵抗値に較正すると共に、第２制御コードに応答して前記第２可変抵抗の抵抗値を前記第１可変抵抗の抵抗値に較正する段階を含むことを特徴とする請求項１に記載の能動終端抵抗の抵抗値較正方法。

【請求項３】 前記第１制御コードを前記第１可変抵抗の抵抗値と前記外部抵抗の抵抗値との比較結果に応じて発生し、前記第２制御コードを前記第１可変抵抗の抵抗値と前記第２可変抵抗の抵抗値との比較結果に応じて発生する段階を備えることを特徴とする請求項２に記載の能動終端抵抗の抵抗値較正方法。

【請求項４】 前記（ａ）段階は、前記第１可変抵抗の抵抗値と前記第２抵抗の抵抗値とが同時に増減する段階を含むことを特徴とする請求項１に記載の能動終端抵抗の抵抗値較正方法。

【請求項５】 能動終端抵抗の抵抗値を較正する方法において、

外部抵抗が接続されるパッドの電圧と基準電圧とを比較してその比較結果に対応する第１比較信号を出力する段階と、

前記第１比較信号に応答して前記パッドの電圧が前記基準電圧と同一になるまで第１可変抵抗の抵抗値を前記外部抵抗の抵抗値に較正する段階と、

前記パッドの電圧と第２可変抵抗の電圧とを比較してその比較結果に対応する第２比較信号を出力する段階と、

前記第２比較信号に応答して第２可変抵抗の抵抗値を前記外部抵抗の抵抗値に較正する段階と、

前記能動終端抵抗の抵抗値を前記第１可変抵抗値及び／又は前記第２可変抵抗の抵抗値に較正する段階とを備えることを特徴とする能動終端抵抗の抵抗値較正方法。

【請求項６】 前記パッドの電圧は、前記第１可変抵抗を通過する電流により生じることを特徴とする請求項５に記載の能動終端抵抗の抵抗値較正方法。

【請求項７】 第２可変抵抗の電圧は、前記第１可変抵抗と同じダミー可変抵抗に流れる電流により生じることを特徴とする請求項５に記載の能動終端抵抗の抵抗値較正方法。

【請求項８】 前記第１可変抵抗の抵抗値と前記第２抵抗の抵抗値とが同時に増減することを特徴とする請求項５に記載の能動終端抵抗の抵抗値較正方法。

【請求項９】 能動終端抵抗の抵抗値を外部抵抗の抵抗値に較正する較正回路において、

外部抵抗が接続される第１ノードの電圧と基準電圧とを比較して、前記第１ノードに電流を供給する第１可変抵抗の抵抗値を制御する第１制御コードを出力する第１制御回路と、

第２可変抵抗が接続される第２ノードの電圧と前記第１ノードの電圧とを比較して、前記第２ノードに電流を供給する前記第１可変抵抗と同じダミー可変抵抗の抵抗値を制御する第２制御コードを出力する第２制御回路とを備え、

前記第１可変抵抗の抵抗値及び前記ダミー可変抵抗の抵抗値は前記第１制御コードに応答して前記外部抵抗の抵抗値に較正されると共に、前記第２可変抵抗の抵抗値は前記第２制御コードに応答して前記外部抵抗の抵抗値に較正され、

前記能動終端抵抗の抵抗値は前記第１制御コード及び／又は前記第２制御コードに応答して前記外部抵抗の抵抗値に較正されることを特徴とする能動終端抵抗の抵抗値較正回路。

【請求項１０】 前記第１可変抵抗の抵抗値と前記第２可変抵抗の抵抗値とは同時に増減することを特徴とする請求項９に記載の能動終端抵抗の抵抗値較正回路。

【請求項１１】 前記第１ノードの電圧は前記第１可変抵抗に流れる電流に応じて生じ、前記第２ノードの電圧は前記ダミー可変抵抗に流れる電流に応じて生じることを特徴とする請求項９に記載の能動終端抵抗の抵抗値較正回路。

【請求項１２】 能動終端抵抗の抵抗値を外部抵抗の抵抗値に較正する較正回路において、

前記外部抵抗及び第１可変抵抗が接続される第１ノードと、

前記第１ノードの電圧と基準電圧とを比較してその比較結果に対応する第１制御コードを出力する第１制御コード発生回路と、

前記第１可変抵抗の抵抗値と同じ抵抗値を有するダミー可変抵抗及び第２可変抵抗が接続される第２ノードと、

前記第１ノードの電圧と前記第２ノードの電圧とを比較してその比較結果に対応する第２制御コードを出力する第２制御コード発生回路とを備え、

前記第１可変抵抗の抵抗値及び前記ダミー可変抵抗の抵抗値は前記第１制御コードに応答して前記外部抵抗の抵抗値に較正されると共に、前記第２可変抵抗の抵抗値は前記第２制御コードに応答して前記外部抵抗の抵抗値に較正され、

前記能動終端抵抗の抵抗値は前記第１制御コード及び／又は前記第２制御コードに応答して前記外部抵抗の抵抗値に較正されることを特徴とする能動終端抵抗の抵抗値較正回路。

【請求項１３】 前記第１可変抵抗の抵抗値と前記第２

可変抵抗の抵抗値とは同時に増減することを特徴とする請求項１２に記載の能動終端抵抗の抵抗値較正回路。

【請求項１４】　前記第１ノードの電圧は前記第１可変抵抗に流れる電流に応じて生じ、前記第２ノードの電圧は前記ダミー可変抵抗に流れる電流に応じて生じることを特徴とする請求項１２に記載の能動終端抵抗の抵抗値較正回路。

【請求項１５】　メモリ装置において、
第１制御コード及び第２制御コードを出力する較正回路と、
選択信号に応答して前記第１制御コード及び前記第２制御コードをマルチプレックシングし、能動終端抵抗の抵抗値を制御するための制御コードを出力するシフトブロックと、
前記制御コードに応答して前記能動終端抵抗の抵抗値を前記較正回路に接続される外部抵抗の抵抗値と一致すべく較正する可変抵抗部とを備え、
前記較正回路は、
前記外部抵抗及び第１可変抵抗が接続される第１ノードと、
前記第１ノードの電圧及び基準電圧を比較してその比較結果に対応する前記第１制御コードを出力する第１制御コード発生回路と、
前記第１可変抵抗の抵抗値と同じ抵抗値を有するダミー可変抵抗及び第２可変抵抗が接続される第２ノードと、
前記第１ノードの電圧及び前記第２ノードの電圧を比較してその比較結果に対応する前記第２制御コードを出力する第２制御コード発生回路とを備え、
前記第１可変抵抗の抵抗値及び前記ダミー可変抵抗の抵抗値は前記第１制御コードに応答して前記外部抵抗の抵抗値に較正されると共に、前記第２可変抵抗の抵抗値は前記第２制御コードに応答して前記外部抵抗の抵抗値に較正されることを特徴とするメモリ装置。

【請求項１６】　前記第１可変抵抗の抵抗値と前記第２可変抵抗の抵抗値とは同時に増減することを特徴とする請求項１５に記載のメモリ装置。

【請求項１７】　前記第１ノードの電圧は前記第１可変抵抗に流れる電流に応じて生じ、前記第２ノードの電圧は前記ダミー可変抵抗に流れる電流に応じて生じることを特徴とする請求項１５に記載のメモリ装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はバスの終端に係り、より詳細には、工程、電圧または温度の変化に関係なく能動終端の抵抗値を較正できる較正回路とその方法及び前記較正回路を備えるメモリ装置に関する。

【０００２】

【従来の技術】一般的に、メモリシステムでバスの終端のためにＳＳＴＬ（ｓｔｕｂ　ｂｕｓＴｅｒｍｉｎａｔｅｄ　ｌｏｇｉｃ）と能動終端（ａｃｔｉｖｅ　ｔｅｒｍｉｎａｔｉｏｎ）とが使われる。能動終端はオンチップ終端（ｏｎ－ｃｈｉｐ　ｔｅｒｍｉｎａｔｉｏｎ）とも言い、チップ内部の能動終端抵抗（以下、「終端抵抗」）を使用してバスの終端を行う。能動終端はＳＳＴＬより信号伝達特性が良く、データレートが高い。

【０００３】終端抵抗の抵抗値（以下、「終端抵抗値」）をいかに正確に所望の抵抗値に較正できるかが能動終端のキーポイントである。従来は、終端抵抗値を較正するための制御信号としてアナログ制御電圧を使用したが、アナログ制御電圧はノイズに敏感なので終端抵抗値を正確に較正できない問題点がある。また、制御電圧がノイズに敏感なので、バスの信号伝達特性が低下する問題点があった。

【０００４】２つのチップを共有して能動終端をする場合（以下、「×２」）、または４つのチップを共有して能動終端をする場合（以下、「×４」）は、一つのチップで能動終端をする場合（以下、「×１」）に比べて終端抵抗値を較正するための他の較正回路が付加的に必要である。従って、従来は、能動終端のための電力消費が増し、レイアウト面積のオーバヘッドがかなり大きい。

【０００５】

【発明が解決しようとする課題】よって、本発明が解決しようとする技術的な課題は、工程、電圧、または温度の変化に鈍感に終端抵抗値を較正できる較正回路とその方法及び前記較正回路を備えるメモリ装置を提供することである。

【０００６】また、本発明が解決しようとする他の技術的な課題は、消費電力とレイアウト面積のオーバヘッド減少させることができる方法及びこれを具現するためのメモリ装置を提供することである。

【０００７】

【課題を解決するための手段】前記技術的な課題を達成するための能動終端抵抗の抵抗値を較正する方法は、（ａ）第１可変抵抗の抵抗値を外部抵抗の抵抗値に較正すると共に第２可変抵抗の抵抗値を前記第１可変抵抗の抵抗値に較正する段階と、（ｂ）前記能動終端抵抗の抵抗値を前記外部抵抗の抵抗値に較正する段階とを備えることを特徴とする。

【０００８】例えば、前記（ａ）段階は、第１制御コードに応答して前記第１可変抵抗の抵抗値を前記外部抵抗の抵抗値に較正すると共に、第２制御コードに応答して前記第２可変抵抗の抵抗値を前記第１可変抵抗の抵抗値に較正する段階を含む。

【０００９】例えば、前記第１制御コードは前記第１可変抵抗の抵抗値と前記外部抵抗の抵抗値との比較結果に応じて生じ、前記第２制御コードは前記第１可変抵抗の抵抗値と前記第２可変抵抗の抵抗値との比較結果に応じて生じるる。

【００１０】例えば、前記（ａ）段階は、前記第１可変抵抗の抵抗値と前記第２抵抗の抵抗値とが同時に増減す

る段階を含む。

【0011】前記技術的課題を達成するための他の能動終端抵抗の抵抗値を較正する方法は、外部抵抗が接続されるパッドの電圧と基準電圧とを比較してその比較結果に対応する第1比較信号を出力する段階と、前記第1比較信号に応答して前記パッドの電圧が前記基準電圧と同一になるまで第1可変抵抗の抵抗値を前記外部抵抗の抵抗値に較正する段階と、前記パッドの電圧と第2可変抵抗の電圧とを比較してその比較結果に対応する第2比較信号を出力する段階と、前記第2比較信号に応答して第2可変抵抗の抵抗値を前記外部抵抗の抵抗値に較正する段階と、前記能動終端抵抗の抵抗値を前記第1可変抵抗値及び／又は前記第2可変抵抗の抵抗値に較正する段階とを備えることを特徴とする。

【0012】例えば、前記パッドの電圧は、前記第1可変抵抗を通過する電流により生じる。

【0013】例えば、前記第2可変抵抗の電圧は、前記第1可変抵抗と同じダミー可変抵抗に流れる電流により生じる。

【0014】例えば、前記第1可変抵抗の抵抗値と前記第2抵抗の抵抗値とは同時に増減する。

【0015】例えば、前記技術的課題を達成するための能動終端抵抗の抵抗値を外部抵抗の抵抗値に較正する較正回路は、外部抵抗が接続される第1ノードの電圧と基準電圧とを比較して前記第1ノードに電流を供給する第1可変抵抗の抵抗値を制御する第1制御コードを出力する第1制御回路と、第2可変抵抗が接続される第2ノードの電圧と前記第1ノードの電圧とを比較して前記第2ノードに電流を供給する前記第1可変抵抗と同じダミー可変抵抗の抵抗値を制御する第2制御コードを出力する第2制御回路とを備え、前記第1可変抵抗の抵抗値及び前記ダミー可変抵抗の抵抗値は前記第1制御コードに応答して前記外部抵抗の抵抗値に較正されると共に、前記第2可変抵抗の抵抗値は前記第2制御コードに応答して前記外部抵抗の抵抗値に較正され、前記能動終端抵抗の抵抗値は前記第1制御コード及び／又は前記第2制御コードに応答して前記外部抵抗の抵抗値に較正されることを特徴とする。

【0016】例えば、前記第1可変抵抗の抵抗値と前記第2可変抵抗の抵抗値とは同時に増減する。

【0017】例えば、前記第1ノードの電圧は前記第1可変抵抗に流れる電流に応じて生じ、前記第2ノードの電圧は前記ダミー可変抵抗に流れる電流に応じて生じることを特徴とする。

【0018】前記技術的課題を達成するための他の能動終端抵抗の抵抗値を外部抵抗の抵抗値に較正する較正回路は、前記外部抵抗及び第1可変抵抗が接続される第1ノードと、前記第1ノードの電圧と基準電圧とを比較してその比較結果に対応する第1制御コードを出力する第1制御コード発生回路と、前記第1可変抵抗の抵抗値と同じ抵抗値を有するダミー可変抵抗及び第2可変抵抗が接続される第2ノードと、前記第1ノードの電圧と前記第2ノードの電圧とを比較してその比較結果に対応する第2制御コードを出力する第2制御コード発生回路とを備え、前記第1可変抵抗の抵抗値と前記ダミー可変抵抗の抵抗値とは前記第1制御コードに応答して前記外部抵抗の抵抗値に較正されると共に、前記第2可変抵抗の抵抗値は前記第2制御コードに応答して前記外部抵抗の抵抗値に較正され、前記能動終端抵抗の抵抗値は前記第1制御コード及び／又は前記第2制御コードに応答して前記外部抵抗の抵抗値に較正されることを特徴とする。

【0019】例えば、前記第1可変抵抗の抵抗値と前記第2可変抵抗の抵抗値とは同時に増減する。

【0020】例えば、前記第1ノードの電圧は前記第1可変抵抗に流れる電流に応じて生じ、前記第2ノードの電圧は前記ダミー可変抵抗に流れる電流に応じて生じる。

【0021】前記技術的課題を達成するためのメモリ装置は、第1制御コード及び第2制御コードを出力する較正回路と、選択信号に応答して前記第1制御コード及び前記第2制御コードをマルチプレックシングし、能動終端抵抗の抵抗値を制御するための制御コードを出力するシフトブロックと、前記制御コードに応答して前記能動終端抵抗の抵抗値を前記較正回路に接続される外部抵抗の抵抗値と一致すべく較正する可変抵抗部とを備え、前記較正回路は、前記外部抵抗及び第1可変抵抗が接続される第1ノードと、前記第1ノードの電圧及び基準電圧を比較してその比較結果に対応する前記第1制御コードを出力する第1制御コード発生回路と、前記第1可変抵抗の抵抗値と同じ抵抗値を有するダミー可変抵抗及び第2可変抵抗が接続される第2ノードと、前記第1ノードの電圧及び前記第2ノードの電圧を比較してその比較結果に相応する前記第2制御コードを出力する第2制御コード発生回路とを備え、前記第1可変抵抗の抵抗値及び前記ダミー可変抵抗の抵抗値は前記第1制御コードに応答して前記外部抵抗の抵抗値に較正されると共に、前記第2可変抵抗の抵抗値は前記第2制御コードに応答して前記外部抵抗の抵抗値に較正されることを特徴とする。

【0022】例えば、前記第1可変抵抗の抵抗値と前記第2可変抵抗の抵抗値とは同時に増減する。

【0023】例えば、前記第1ノードの電圧は前記第1可変抵抗に流れる電流に応じて生じ、前記第2ノードの電圧は前記ダミー可変抵抗に流れる電流に応じて生じる。

【0024】

【発明の実施の形態】以下、添付した図面を参照して本発明の望ましい実施形態を説明することにより、本発明を詳細に説明する。各図面に提示された同じ参照符号は同じ構成要素を示す。

【0025】図1は 本発明の望ましい実施形態の能動

終端抵抗較正回路を備えるメモリ装置のブロック図を概略的に示す。図1を参照すれば、チップ100は、能動抵抗較正回路（以下、「較正回路」）20、シフトブロック30、多数の可変抵抗部40と多数のパッド50，60，70を備える。較正回路20は、パッド10を通じて外部抵抗Ｒｅｘｔと接続される。

【0026】較正回路20は、第1制御コードUPCODE及び第2制御コードDNCODEをシフトブロック30に出力する。第1制御コードUPCODE及び第2制御コードDNCODEは、例えばNビットで構成される。

【0027】シフトブロック30は、複数のシフタ31を備えており、選択信号SELに応答し、×1，×2または×4のための終端抵抗値を制御する制御コードHCODE_Ui，HCODE_Di（ここでiは1ないし3）を複数の可変抵抗部40に出力する。制御コードHCODE_Ui，HCODE_Diは、例えばNビットで構成される。

【0028】従って、シフタ31は、第1／第2制御コードUPCODE／DNCODEを1回またはそれ以上シフトさせて、×2または×4のための終端抵抗値を発生させることができるという長所がある。

【0029】複数の可変抵抗部40のそれぞれは、第1可変抵抗41と第2可変抵抗43とを備え、制御コードHCODE_Ui，HCODE_Diに応答して終端抵抗値を外部抵抗Ｒｅｘｔの抵抗値と一致させるように較正する。パッド50は、例えばデータ出力のためのパッドであり、パッド60は、例えばクロック信号のためのパッドであり、パッド70は、例えばアドレス／命令信号のためのパッドである。複数のパッド50，60，70のそれぞれは、複数の可変抵抗部40それぞれのノードN1に接続される。

【0030】図2は、本発明の望ましい実施形態の較正回路の回路図を示す。図2を参照すれば、較正回路20は、第1可変抵抗41とダミー可変抵抗42、第2可変抵抗43、2つの比較回路21，23、第1制御コード発生回路25及び第2制御コード発生回路27を備える。

【0031】第1可変抵抗41は、第1電源VDDQとパッド10との間に接続され、ダミー可変抵抗42は、第1電源VDDQとノードN3との間に接続され、第2可変抵抗43は、ノードN3と第2電源VSSQとの間に接続される。ダミー可変抵抗42の構造及び動作は、第1可変抵抗41の構造及び動作と同一であり、ダミー可変抵抗42と第2可変抵抗43とは、図5に示されたように互いに対称的な構造を有するが、その動作は同一である。

【0032】比較回路21は、基準電圧VREFとパッド10の電圧とを比較して、その比較結果に対応する第1比較信号UP_COMPを第1制御コード発生回路25に出力する。パッド10の電圧は、第1可変抵抗41に流れる電流により変化する。

【0033】比較回路23は、ノードN3の電圧とパッド10の電圧とを比較して、その比較結果に対応する第2比較信号DN_COMPを第2制御コード発生回路27に出力する。ノードN3の電圧は、ダミー可変抵抗42を通じて流れる電流により変化する。基準電圧VREF及びノードN3の電圧は、0．5VDDQであることが望ましい。

【0034】第1制御コード発生回路25は、第1比較信号UP_COMPに応答して第1制御コードUPCODEを第1可変抵抗41、ダミー可変抵抗42及びシフトブロック30に出力する。第1可変抵抗41の抵抗値及びダミー可変抵抗42の抵抗値が第1制御コードUPCODEに応答して外部抵抗Ｒｅｘｔの抵抗値と同一に較正される場合、基準電圧VREFとパッド10の電圧とは同一になる。第1制御コード発生回路25は、一般的なアップ／ダウンカウンタで構成されるので詳細な説明は省略する。

【0035】第2制御コード発生回路27は、第1比較信号UP_COMP及び第2比較信号DN_COMPに応答して、第2制御コードDNCODEを第2可変抵抗43とシフトブロック30とに出力する。第2可変抵抗43の抵抗値が第2制御コードDNCODEに応答してダミー可変抵抗42の抵抗値と同一に較正される場合、ノードN3の電圧とパッド10の電圧とは同一になる。

【0036】図3は、図2の第2制御コード発生回路のブロック図を示す。図3を参照すれば、第2制御コード発生回路27は、論理ゲート28とアップ／ダウンカウンタ29とを備える。論理ゲート28は、否定排他的論理和演算（Ｅｘｃｌｕｓｉｖｅ－NOR）回路であり、アップ／ダウンカウンタ29は、論理ゲート27の出力信号に応答してイネーブルされる。すなわち、アップ／ダウンカウンタ29は、第1状態（または、第2状態）を有する第1比較信号UP_COMPと第2比較信号DN_COMPとに応答してイネーブルされるため、デジタル較正により生じる量子化誤差は減少する。

【0037】図1ないし図3を参照して第1可変抵抗41の抵抗値と第2可変抵抗43の抵抗値とが外部抵抗Ｒｅｘｔの抵抗値に一致するように較正される場合を説明する。

【0038】まず、パッド10の電圧は、第1可変抵抗41に流れる電流により決定され、パッド10の電圧が基準電圧VREFより大きい場合（すなわち、第1可変抵抗41の抵抗値が外部抵抗Ｒｅｘｔの抵抗値より小さい場合）、比較回路21は第1状態の第1比較信号UP_COMPを出力し、アップ／ダウンカウンタで構成される第1制御コード発生回路25は第1状態の第1比較信号UP_COMPに応答してダウンカウンティングするので、第1制御コードUPCODEは減少する。

【0039】従って、第1可変抵抗41の抵抗値及びダミー可変抵抗42の抵抗値は、第1制御コードUPCODEに応答して増加する。このような動作は、パッド10の電圧と基準電圧VREFとが同一になるまで反復的に行われるので、結局、第1可変抵抗41の抵抗値及びダミー可変抵抗42の抵抗値が外部抵抗Rextの抵抗値に一致すように較正される。

【0040】パッド10の電圧が基準電圧VREFより小さい場合（すなわち、第1可変抵抗41の抵抗値が外部抵抗Rextの抵抗値より大きい場合）、比較回路21は第2状態の第1比較信号UP_COMPを出力し、第1制御コード発生回路25は第2状態の第1比較信号UP_COMPに応答してアップカウンティングするので、第1制御コードUPCODEは増加する。

【0041】従って、第1可変抵抗41の抵抗値及びダミー可変抵抗42の抵抗値は、第1制御コードUPCODEに応答して減少する。このような動作は、パッド10の電圧と基準電圧VREFとが同一になるまで反復的に行われるので、結局、第1可変抵抗41の抵抗値及びダミー可変抵抗42の抵抗値が外部抵抗Rextの抵抗値に一致するように較正される。

【0042】次に、ノードN3の電圧はダミー可変抵抗42に流れる電流により決定され、パッド10の電圧がノードN3の電圧より大きい場合（すなわち、第2可変抵抗43の抵抗値が第1可変抵抗41またはダミー可変抵抗42の抵抗値より小さい場合）、比較回路23は第1状態の第2比較信号DN_COMPを出力する。

【0043】第2制御コード発生回路27は、第1状態の第1比較信号UP_COMPと第1状態の第2比較信号DN_COMPとに応答してダウンカウンティングされた第2制御コードDNCODEを第2可変抵抗43に出力するので、第2可変抵抗43の抵抗値は、第2制御コードDNCODEに応答してダミー可変抵抗42の抵抗値と同一になるまで増加する。

【0044】パッド10の電圧がノードN3の電圧より小さい場合（すなわち、第2可変抵抗43の抵抗値がダミー可変抵抗42の抵抗値より大きい場合）、比較回路23は、第2状態の第2比較信号DN_COMPを出力する。第2制御コード発生回路27は、第2状態の第1比較信号UP_COMPと第2状態の第2比較信号DN_COMPとに応答してアップカウンティングされた第2制御コードDNCODEを第2可変抵抗43に出力するので、第2可変抵抗43の抵抗値は、第2制御コードDNCODEに応答してダミー可変抵抗42の抵抗値と同一になるまで減少する。

【0045】すなわち、前述の過程を通じて、較正回路20は、工程、電圧または温度に関係なく可変抵抗41，42及び43の抵抗値を同時に増減させるので、可変抵抗41，42及び43の抵抗値は、外部抵抗Rextの抵抗値に較正される。また、比較回路21，23にオフセットがある場合にも、前述の過程によりパッド10の電圧とノードN3の電圧と基準電圧VREFとは同一になる。

【0046】すなわち、本発明の望ましい実施形態の較正回路20は、比較器21，23のオフセットによる終端電圧の変化を補償できるので、高速動作時のタイミングマージンを増加させることができる。

【0047】図4は、図1のシフタの回路図を示す。図4を参照すれば、シフタ31は、複数のマルチプレックサ33を備える。マルチプレックサ33は、Nビットの選択信号SELに応答して、第1／第2制御コードUPCODE／DNCODEをマルチプレックシングし、×1，×2または×4のための終端抵抗値を制御する制御コードHCODE_UiとHCODE_Di（ここでiは1ないし3）を出力する。

【0048】×2の場合、シフタ#3，#4は選択信号SELに応答して第1／第2制御コードUPCODE／DNCODEに同じ制御コードHCODE_U2／HCODE_D2を出力する一方、シフタ#5，#6は選択信号SELに応答して第1／第2制御コードUPCODE／DNCODEを1回シフトした制御コードHCODE_U3／HCODE_D3を出力する。

【0049】図5は、図1の可変抵抗部の回路図を示す。第1可変抵抗41及びダミー可変抵抗42は、複数のPMOSトランジスタと複数の抵抗R，2^1R，2^2R，．．．，2^NRを備え、それぞれのトランジスタはそれぞれの抵抗と直列に接続される。制御コードHCODE_Ui，HCODE_Di（ここで、iは1ないし3）は、2進で重み付けされたコードであり、対応するトランジスタのゲートに入力される。それぞれの抵抗は、図5に示されたように重み付けされた抵抗値を有する。

【0050】第1可変抵抗41及びダミー可変抵抗42は、制御コードHCODE_Ui，HCODE_Di（ここで、iは1ないし3）に対応した抵抗値を有する抵抗として機能する。すなわち、×1の抵抗値、×2の抵抗値、×4の抵抗値は互いに異なる。

【0051】第2可変抵抗43は、複数のNMOSトランジスタと複数の抵抗R，2^1R，2^2R，．．．，2^NRを備え、それぞれのトランジスタはそれぞれの抵抗と直列に接続される。制御コードHCODE_Di，HCODE_Di（ここで、iは1ないし3）は2進で重み付けされたコードであり、対応するトランジスタのゲートに入力される。それぞれの抵抗は図5に示されたように重み付けされた抵抗値を有する。

【0052】本発明の望ましい実施形態のチップ100は、一つの較正回路20とシフタ31とを使用して第1／第2制御コードUPCODE／DNCODEをシフトさせ、×2または×4のための終端抵抗値を同時に発生させることができる。よって、本発明の望ましい実施形

態のチップ１００は、消費電力を減少させることができるという長所があり、また、レイアウト面積のオーバヘッドを減少させることができるという効果がある。

【００５３】本発明は、図面に示された望ましい実施形態を参考に説明されたが、これは例示的なものに過ぎず、本技術分野の当業者ならばこれから多様な変形及び均等な他の実施形態が可能であるという点を理解できるであろう。従って、本発明の真の技術的保護範囲は特許請求範囲の技術的思想により決まるべきである。

【００５４】

【発明の効果】本発明による較正回路及び較正法は、工程、電圧、または温度に関係なく終端抵抗の抵抗値を較正することができるという長所がある。

【００５５】そして、本発明による較正回路及び較正方法は、ノイズに対する耐性を強めることができるという長所がある。そして、本発明による較正回路及び較正方法は、バスの終端を容易に制御することができるという長所がある。

【００５６】また、本発明による較正回路及び較正方法は、デジタル制御による量子化誤差を減少させることができる。さらに、本発明によるメモリ装置は、消費電力を減少させ、高速動作時のタイミングマージンを大きくでき、レイアウト面積のオーバヘッドを減少させることができるという長所がある。

【図面の簡単な説明】

【図１】本発明の望ましい実施形態の較正回路を備えるメモリ装置のブロック図を概略的に示す。

【図２】本発明の望ましい実施形態の較正回路の回路図を示す。

【図３】図２の第２制御コード発生回路のブロック図を示す。

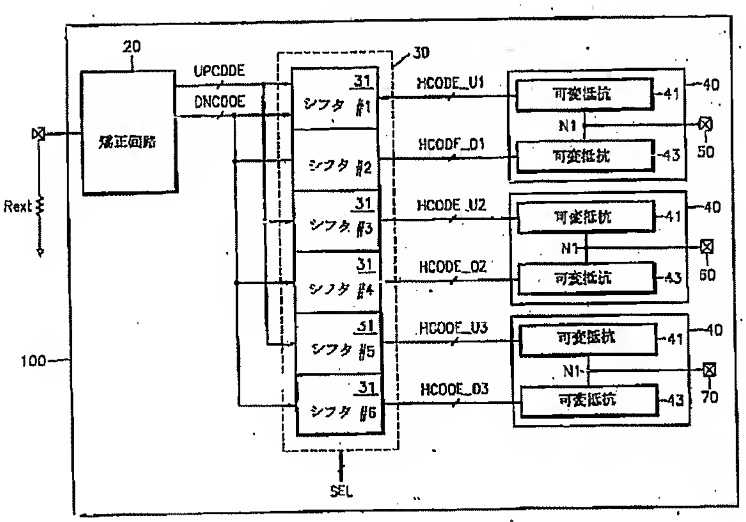
【図４】図１のシフタの回路図を示す。

【図５】図１の可変抵抗部の回路図を示す。

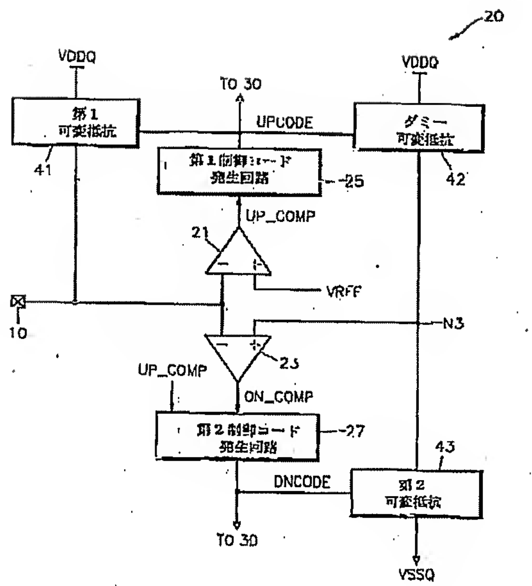
【符号の説明】

２０　能動抵抗較正回路
３０　シフトブロック
３１　シフタ
４０　可変抵抗部
４１　第１可変抵抗
４３　第２可変抵抗
５０，６０，７０　パッド
１００　チップ

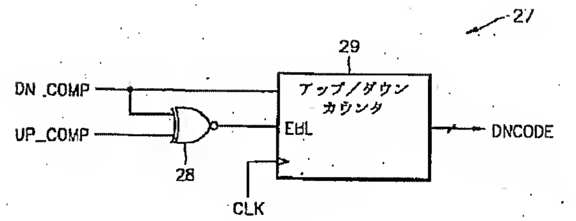
【図１】



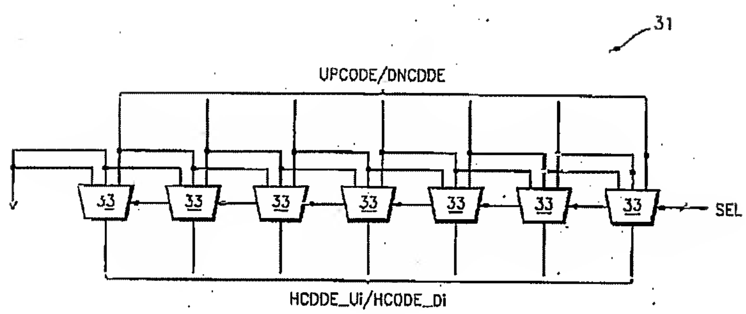
【図2】


20
VDDQ
第1
可変抵抗
41
TO 30
UPCODE
VDDQ
ダミー
可変抵抗
42
第1制御コード
発生回路
25
UP_COMP
21
VREF
10
N3
23
UP_COMP
DN_COMP
第2制御コード
発生回路
27
43
DNCODE
第2
可変抵抗
TO 30
VSSQ

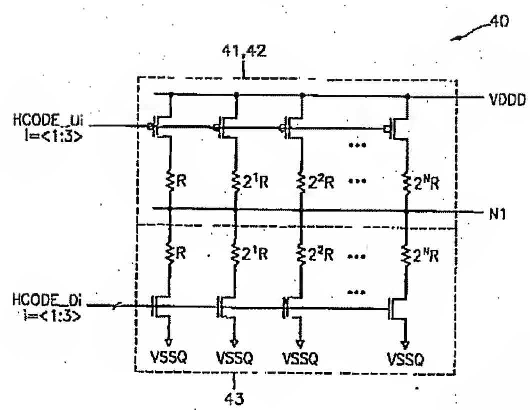
【図3】


27
29
DN_COMP
UP_COMP
アップ/ダウン
カウンタ
EBL
DNCODE
28
CLK

【図4】


31
UPCODE/DNCODE
33
SEL
HCODE_Ui/HCODE_Di

【図5】



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